UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,154	09/08/2003	Mark L. Burgener	PER-005-PAP	5658

7590 05/17/2007

JAQUEZ & ASSOCIATES
Suite 1000
6265 Greenwich Drive
San Diego, CA 92122-5916

EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
05/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/658,154	BURGENER ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2006 and 08 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11,21,42 and 52* is/are allowed.

6)☒ Claim(s) *1-10,12-20,22-25,27-41,43-51 and 53-67* is/are rejected.

7)☒ Claim(s) *26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20060515*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Appeal Brief

In view of the Appeal Brief filed on Jan 8, 2007, PROSECUTION IS HEREBY REOPENED.

New rejections, and modified versions of some previous rejections, are set forth below. Therefore, this Office Action is **NON-FINAL**.

To avoid abandonment of the application, the appellants must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then the appellants must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

After considering the applicants' arguments/comments within the Appeal Brief filed on Jan 8, 2007, and then reconsidering the claim language and objections/rejections described in the previous Office Action, all those objections and rejections have now been withdrawn to minimize confusion with respect to present Office Action's objections/rejections. Therefore, this

Office Action is **NON-FINAL** and describes new, and/or modified, objections and rejections later under the appropriate section, wherein these objections/rejections are deemed the most relevant with respect to understanding the claimed limitations, and of the prior art references one of ordinary skill in the art would be familiar with. Also, related comments by the examiner are described under the Response to Arguments section.

Claim Objections

Claims 46-47, 51, and 62 are objected to because of the following informalities: For consistent labeling throughout the claims, it is suggested: 1) "the discharging switch" on line 2 of both claims 46 and 47 be changed to --the discharging switch circuit-- to relate back to "discharging switch circuit" cited on line 3 of claim 43; 2) "a voltage source" on the first line of claim 51 should be changed to --the voltage source-- to relate back to "a voltage source" in the preamble of claim 49; and 3) "the switch device" on line 2 of claim 62 should be --the switch-- to more clearly relate back to the "charging switch" and the "discharging switch" cited on lines 4,6 and 8,11, respectively of claim 60. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10, 12-17, 19-20, and 28-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. The phrasing "an odd number of not more than three inverting driver sections cascaded sequentially" in lines 5-6 of claim 1 is confusing. For example, since this implies the ring oscillator can have just one (i.e. an odd number) section,

how can that section be "cascaded sequentially", and/or coupled to the next section that does not exist? Also, where is the applicants' support that shows or discloses a ring oscillator having only one section, and how that one section oscillator actually operates? Clarification is requested with respect to what is meant by "coupling substantial charge into the transfer capacitor via the charge pump clock input" as cited in claim 10. For example, does this imply that the charge actually comes from the charge pump clock output, or does this refer to a conducting state of at least one of the transfer capacitor coupling switches, wherein the charge into the capacitor is actually through the coupling switch? Using the applicants' own Fig. 6 as an example, is transfer capacitor 606 actually charged via Vin+ through 602 when it's conducting, or is it charged by CLK? For example, does it refer to an average of the clock output, the output supply, or the source voltage? Claim 19 cites "a second charge pump stage", thus implying a "first charge pump stage" that has not been clearly identified within the claim's chain of dependency. Related to this, it is not clear within the claims how the implied first stage from claim 19 relates to the switching devices and charge pump clock generating circuit cited within claim 18. The phrasing "substantially sine-like" in claims 12 (line 9), 20 (line 3), and 28 (line 10) is relative, rendering the claims, and their corresponding dependent claims (if any), indefinite. The phrase is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, one of ordinary skill in the art would not be reasonably apprised of the scope of the invention, and the applicants' previous comments have never clearly described what it actually means. For example, until the applicant clearly defines what is meant by "substantially sine-like", this examiner will assume that any signal that is not a true square (or rectangular) wave that has sharp rising and falling edges (e.g. no, or at least minimal, transition times) will be

considered "substantially sine-like"? These signals would include those that have at least one rising or falling edge that gradually changes in either a linear or non-linear manner (e.g. the transition between a logic high level and a logic low level is not substantially instantaneous). It is not clear what "an average voltage" relates to on lines 2-3 of claim 62.

Claim 13 recites the limitation "the driver output node" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 43 recites the limitation "the driver circuit" in line 8 with an insufficient antecedent basis for this limitation in the claim.

Claim 60 recites the limitation "the output from a source voltage" in line 2. There is insufficient antecedent basis for this limitation in the claim. For example, is this phrasing referring to a source voltage output that has not been clearly identified before, or to the "output supply" cited on line 1?

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 18-19, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imamiya, one reference found during a recent search, in view of Pfiffner. Fig. 15B of Imamiya shows a charge pump apparatus for generating output voltage supply at the common connection of C2 and QN12 of section 51-2, wherein section 51-1 of the apparatus comprises transfer capacitor C2; source switching device QN11 is between transfer capacitor C2 and voltage source VDD to transfer current from voltage source VDD when QN11 is conducting; output switching device QP12 is between transfer capacitor C2 and the output voltage supply OUT to transfer current from transfer capacitor C2 to the output voltage supply when QP12 is conducting; and it would be obvious to one of ordinary skill in the art that a charge pump clock generating circuit (e.g. clock generator 2 shown in Fig. 2 and disclosed as a ring oscillator for generating at least clock output Ø on column 4, lines 49-51) would be configured to generate single-phase charge pump clock output Ø coupled passively to the control node of source switching device QN11 of section 51-1 to cause conduction during charge periods (i.e. when Ø is high) and nonconduction during discharge periods (i.e. when Ø is low), and also be coupled passively to the control node of output switching device QP12 of section 51-1 to cause nonconduction during charge periods (i.e. when Ø is high) and conduction during discharge periods (i.e. when Ø is low), wherein the charge periods will alternate with, and do not overlap, the discharge periods due to the known operation of PMOS and NMOS transistors receiving the same clock output Ø signal. Since clock

output Ø is coupled to the gates of QN11 and QP12, no substantial transfer current will be conveyed (i.e. MOS transistors are voltage controlled devices, and no substantial current will flow through their gate to their source or drain). Clock output Ø is passively coupled to the control nodes via the interconnecting line connecting the output of the charge pump clock generating circuit and the control nodes. For example, Pfiffner discloses "passive elements are...interconnect lines" on column 1, lines 44-45. Therefore, claim 18 is rendered obvious. Unless full voltage regulation and detecting are required, one of ordinary skill in the art would understand that the use of Fig. 2's R1, R2, CMP, 904, and 903 would not be necessary, and therefore the output of oscillator 902 would be applied to the input of charge pump 901 directly. The apparatus shown within Fig. 15B also shows second charge pump stage 51-2 comprising second transfer capacitor C2; second source switching device QN11 disposed between transfer capacitor C2 and voltage source VDD; and second output switching device QP12 is between transfer capacitor C2 and second output voltage supply OUT, wherein charge pump clock output Ø is coupled to both QN11 and QP12, wherein second source switching device QN11 of section 51-2 will conduct during charge periods (i.e. when Ø is high) and be nonconductive during discharge periods (i.e. when Ø is low), and second output switching device QP12 of section 51-2 will be nonconductive during charge periods (i.e. when Ø is high) and conductive during discharge periods (i.e. when Ø is low). This renders claim 19 obvious. In Fig. 15A, Imamiya's TC discharging switch QP11, under control of single phase charge pump clock output Ø, couples TC C2 to output supply OUT during discharge periods (i.e. when Ø is low); and TC charging switch QN11, during charge periods (i.e. when Ø is high) that nonoverlappingly alternate with the discharge periods, and also under control of single-phase charge pump clock output Ø,

couples TC C2 to voltage source VDD. Single-phase charge pump clock output Ø is passively coupled to the control node (e.g. gate) to TC discharging switch QP11 and TC charging switch QN11 because there is no intervening element between single phase charge pump clock Ø and Imamiya's control node, wherein an interconnecting line is one known type of passive element. For example, Pfiffner discloses "the only passive elements are...interconnect lines" on column 1, lines 44-45. This interpretation of passive coupling renders claim 49 obvious.

Claims 1-4, 9-10, 12-14, 16-17, 28-33, 36-41, 43-45, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imamiya, one reference found doing a recent search, in view of Ito et al. (Ito), a reference cited in previous Office Actions. Imamiya shows a charge pump apparatus in Fig. 15A that generates output voltage supply OUT, and comprises transfer capacitor C2, and a plurality of transfer capacitor coupling switches QN11-QN12,QP11-QP12, each switchable between a conducting state and a nonconducting state under control of at least charge pump clock output Ø, wherein during periodic first times (e.g. Ø is high), transfer capacitor C2 is coupled to voltage source VDD through transfer capacitor coupling switch QN11, and during periodic second times (e.g. Ø is low) that are not concurrent with the first times, transfer capacitor C2 is coupled to output voltage supply OUT through transfer capacitor coupling switch QP11. Although Fig. 15A does not clearly show a charge pump clock generating circuit, that provides charge pump clock output Ø, as a ring oscillator with three driver sections including circuitry to limit the rise and fall of each of the driver section's output, Imamiya does disclose the relationship between clock signals and an oscillator, such as a ring oscillator, for generating at least clock output Ø (e.g. see column 1, lines 36-37; and column 4, lines 49-51). Therefore, one of ordinary skill in the art would understand that charge pump clock output Ø,

used to control the plurality of transfer capacitor coupling switches of Imamiya, would be provided by some type of a charge pump clock generating circuit, such as ring oscillator. Ito shows and discloses various examples of ring oscillators that provide a clock output. Therefore, it would have been obvious to one of ordinary skill in the art to utilize Ito's ring oscillator 70 (shown in Fig. 12) as the charge pump clock generating circuit/(ring) oscillator that provides charge pump clock output Ø to control Imamiyu's plurality of transfer capacitor coupling switches. Ito's ring oscillator comprises three inverting driver sections (i.e. 59,51a,51b,62; 60,52a,52b,63; and 61,53a,53b,64) cascaded sequentially in a ring, wherein driver section 61,53a,53b,64 outputs charge pump clock output CLKO, which would correspond to Imamiyu's charge pump clock output Ø. Each stage comprises circuitry to limit the rate of rise and fall of voltage at the driver section's output. For example, driver section 61,53a,53b,64 includes: 1) circuitry 61,53a configured as an active current limit to limit the rate of rise of voltage CLKO from a low level to a high level when 53a is turned on, and circuitry 53b,64 configured as an active current limit to limit the rate of fall of voltage CLKO from a high level to a low level when 53b is turned on. This renders claim 1 obvious. The use of Ito's ring oscillator is just one example of a ring oscillator that would provide stable generation of charge pump clock output Ø (i.e. Ito's CLKO). Since each transfer capacitor coupling switch is controlled by charge pump clock output CLKO/Ø, claim 2 is rendered obvious. Deeming the line coupling the clock output from Ito's charge pump clock generating circuit 70 to each of Imamiya's transfer capacitor coupling switches QN11-QN12, QP11-QP12 as coupling circuitry, the signal will be coupled to each coupling switch without increasing the rise of voltage rise or fall, thus rendering claims 3-4 obvious. The current mirror configurations shown in Ito's Fig. 12, which limits source and sink

currents conducted by each driver section, will ensure substantially identical magnitudes. For example, the sink currents through transistors 62-64 will correspond to the currents flowing within transistors 56-57, and the source currents through transistors 59-61 will correspond to the current flowing within transistor 58. With transistors 58 and 57 coupled in series between Vdd and Vss, their currents will be the same, and claim 9 is rendered obvious. Since transfer capacitor C2 will be periodically coupled between voltage source VDD and ground in response to charge pump clock output Ø in order to charge, a substantial charge will be coupled into transfer capacitor C2 through QN11 during those periods, and with the conducting state of QN11 controlled by output Ø, the charge will be effectively via charge pump clock output Ø, thus rendering claim 10 obvious. In another interpretation of Imamiya's Fig. 15A, one of ordinary skill in the art would realize active switches QN11 and QN12 allow transfer capacitor C2 to be charged, and active switches QP12 and QP11 allow transfer capacitor C2 to be discharged in an alternating, non-overlapping, manner. This would allow transfer capacitor C2 to be coupled alternately between source connection VDD and output connection OUT. Ito's charge pump clock generating circuit 70 comprises active driver circuit 70 configured to source current (via 61,53a) to, and sink current (via 53b,64) from, charge pump clock output CLKO (of Ito, corresponding to Imamiya's Ø). The periodic switching of 61,53a and 53b,64 will effectively provide a waveform that is substantially sine-like (e.g. not a true square wave) due to the current limiting of 61 and 64, and capacitance 53c. Since clock output CLKO/Ø will be coupled to the gates of Imamiya's MOS transistors QN11-QN12,QP11-QP12 (the plurality of active switches), there will be no substantial charge from clock output CLKO/Ø that is coupled from source connections VDD to output connections OUT of transfer capacitor C2. Imamiya's circuitry

61,53a will limit the source current provided by active driver circuit 70 to clock output CLK0/Ø, and circuitry 53b,64 will limit the current sunk from clock output CLKO/Ø, rendering claim 12 obvious. Discrete capacitive element 53c of Ito's charge pump clock generating circuit 70 is coupled to driver output node CLKO, and this will reduce voltage rates of change at that node, rendering obvious claim 13. Since charge pump clock generating circuit 70 includes a plurality of active driver circuits (e.g. 51a,51b; 52a,52b; and 53a,53b) configured to both source and sink current with respect to a corresponding driver output node, wherein circuitry 59-61 limits the current source capacity to each active driver circuit, and circuitry 62-64 limits current sink capacity in each active driver circuit, and claim 14 is rendered obvious. Charge pump clock generating circuit 70 of Ito is a current-starved ring oscillator, and claim 16 is rendered obvious. For the same type of reasoning as applied to claim 9 described above, claim 17 is also rendered obvious since the source current circuitry and sink current circuitry are configured to limit source and sink currents to a substantially identical magnitude. In another interpretation of the Imamiya/Ito combination, Imamiya's discharging TCCS circuit QP11 couples transfer capacitor (TC) C2 to output supply OUT during discharge periods under control of first charge pump clock output CLKO/Ø (i.e. when its low); and Ito's 61,53a,53b,64 actively limit a rate of voltage change of the first charge pump clock output CLKO/Ø during both positive and negative transitions such that a voltage of first charge pump clock output CLKO/Ø is substantially sine like (e.g. not a true square wave), rendering claim 28 obvious. Imamiya's charging TCCS circuit QN11 couples transfer capacitor (TC) C2 to source voltage VDD during charge periods under control of second charge pump clock output CLKO/Ø (i.e. when its high) that nonoverlappingly alternate with the discharge periods (e.g. when one is high, the other is low); and Ito's

61,53a,53b,64 actively limit a rate of voltage change of the second charge pump clock output CLKO/Ø, and claim 29 is rendered obvious. Since the first/second charge pump clock outputs correspond to charge pump clock output CLKO/Ø, they are the same clock output, rendering claim 30 obvious. Also, all TCCS circuits QN11-QN12,QP11-QP12 are controlled by means of charge pump clock output CLKO/Ø, and they are all controlled by the first charge pump clock output, rendering claim 31 obvious. When TCCS circuit QN11 is conducting, TC C2 is connected to source voltage VDD during the charging period via charge pump clock output CLKO/Ø. Therefore, claim 32 is rendered obvious. Ito's current limiting circuit 61,53a, 53b,64 limits current drive capacity of charge pump clock output CLKO/Ø, rendering obvious claim 33. Ito's first clock generator driver circuit 61,53a,53b,64 is a driver circuit functionally incorporated in first clock generator circuit 70, which is configured to generate first charge pump clock output CLKO/Ø. First current limiting circuit 61,53a limits source currents from particular first clock generator driver circuit 61,53a,53b,64; and second current limiting circuit 53b,64 limits sink currents into the particular first clock generator driver circuit, rendering claim 36 obvious. Due to the current mirror relationships of 61 and 64 with 56-58, the source and sink currents will be limited to substantially identical magnitudes, and claim 37 is rendered obvious. First current limiting circuit 61,53a comprises current mirror device 61 (e.g. with respect to current mirror 58-61), and second current limiting circuit 53b,64 comprises different current mirror device 64 (e.g. with respect to current mirror 56-57,62-64), thus rendering obvious claim 38. 59-61 limit source currents, and 62-64 limit sink currents, from all first clock generator driver circuits (e.g. 51a,51b; 52a,52b; and 53a,53b), and claim 39 is rendered obvious. Since Ito's first charge pump clock output CLKO/Ø is generated by means of current-starved ring oscillator 70, that includes three

inverting driver sections 59,51a,51b,62; 60,52a,52b,63; and 61,53a,53b,64 coupled in a ring, claim 40 is also rendered obvious. When conducting and not in any transitioning phase, TCCS circuit QN11 couples TC C2 to source voltage VDD passively, and TCCS circuit QP11 couples TC C2 to output supply OUT. Therefore, under these conditions (i.e. conducting, and not transitioning), QN11 and QP11 will each be one type of a passive TCCS circuit, rendering claim 41 obvious. In another interpretation of the Imamiya/Ito combination, discharging switch circuit QP11 couples TC C2 to output supply OUT under control of first charge pump clock output CLKO/Ø (i.e. when low); corresponding source current limiting circuits 59-61 limit source current provided to each corresponding driver output node within current-starved ring oscillator 59,51a,51b,62/60,52a,52b,63/61,53a,53b,64 having three inverting driver stages (e.g. the first stage comprises 59,51a,51b,62); corresponding sink current limiting circuits 62-64 limit sink current drawn from each corresponding driver output node; and inverting driver output node CLKO of inverting driver stage 61,53a,53b,64 of the first charge pump clock generator is first charge pump clock output CLKO/Ø, rendering claim 43 obvious. TC C2 is coupled to source voltage VDD via charging switch circuit QN11, under control of second charge pump clock output CLKO/Ø (i.e. when high), during charge periods alternating nonconcurrently with the discharge periods (e.g. only of QN11 and QP11 is on at a time), and claim 44 is rendered obvious. Capacitor 53c is coupled to driver output node CLKO of the first charge pump clock generating circuit to limit voltage transition rates of driver output node, rendering claim 45 obvious. The connecting line between first charge pump output CLKO/Ø and the control node (e.g. gate) of discharging switch circuit QP11 is one type of network (e.g. a network of a single line) that is not configured to increase rates of voltage change of the signal, and claim 48 is

rendered obvious. [Note: The rates of voltage change are determined by the current limiting within 70.]

Claims 3-8, 15, 18, 22-23, 34-35, 46-49, and 54-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imamiya/Ito as applied to their corresponding claim 1, 12, 28 or 43 above, and further in view of Yamashiro, another reference found during a recent search. As previously described, the combination of Imamiya/Ito reads on the limitations recited within the basic claims. However, neither of those references clearly shows or discloses a capacitive coupling circuit configured to couple the charge pump clock output to a control node of at least one, or of each, transfer capacitor coupling switch. Fig. 1 of Yamashiro shows an example for coupling one single input signal Vin to the control node of a pair of coupling switches Mn,Mp, and discloses these capacitors are for AC coupling and DC blocking with respect to sine like waves of an oscillating operation (e.g. see column 3, lines 9-12 and 55-66). Therefore, it would have been obvious to one of ordinary skill in the art to add a corresponding capacitive coupling circuit between clock output CLKO of Ito's charge pump clock generating circuit 70 (corresponding to clock output Ø of Imamiya's circuit) and the control node of each of the plurality of transfer capacitor coupling switches QN11-QN12,QP11-QP12 of Imamiya's circuit, rendering claims 3-6 obvious, wherein capacitive coupling is one known type of coupling circuitry. Use of coupling (or blocking) capacitors are well known to those of ordinary skill in the art, and these capacitive coupling circuits will block any unnecessary DC component from Ito's charge pump clock generating circuit 70, while still allowing the AC component of clock output CLKO/Ø to control Imamiya's transfer capacitor coupling switches. This would minimize any inaccurate triggering of the coupling switches due to unwanted DC biasing. Since

none of these capacitive coupling circuits would directly conduct substantial charge to transfer capacitor C2, claims 7-8 are also rendered obvious. For the same type of reasoning as applied to claims 3-6 above, claims 15, 34-35, and 46-47 are rendered obvious. However, it is noted that the transfer capacitor coupling switches of claims 5-6 are now identified as: 1) active switch(es) within claim 15; 2) TCCS circuits within claims 34-35; and 3) discharging (or charging) switches within claims 46-47. Also, the capacitive coupling switches of claims 5-6 are now identified as capacitive coupling networks within claim 15. The corresponding capacitive coupling circuit is one type of network that couples clock output Ø to the control nodes of the discharging switch circuit QP11, it will not be configured to increase rates of voltage change of the signal, and claim 48 is rendered obvious. The rate increase will actually depend on Ito's current limiting abilities. Also, this capacitive coupling is one type of passive coupling, rendering claim 18 obvious. Since Ito's circuitry 59-61 and 62-64 limit currents by each amplifier driver circuit (e.g. 51a,51b; 52a,52b; and 53a,53b), claim 22 is rendered obvious. Ito's discrete capacitive device 53c renders claim 23 obvious. For the same type of reasoning previously presented above, claims 49 and 56-59 are also rendered obvious. Also, although Fig. 15A of Imamiya shows only a single stage for generating an output supply, Fig. 15B shows two stages 51-1 and 51-2, wherein one of ordinary skill in the art would understand section 51-1 closely corresponds to Fig. 15A with OUT and QP11 of Fig. 15A now corresponding to the common connection between C2 and QN12, and to QP12 coupled to that common connection. Therefore, one of ordinary skill in the art would also understand second TC C2 (of section 51-2) would be coupled to second voltage source VDD via second TC charging switch QN11 (of section 51-2) under control of clock output CLKO/Ø, and second TC C2 (of section 51-2) is coupled to second output supply OUT via second TC

discharging switch QP11 (of section 51-2) that is also under control of clock output CLKO/Ø, rendering obvious claim 54. It would also have been obvious to one of ordinary skill in the art to couple clock output CLKO/Ø to the control node of each TC charging switch, and each TC discharging switch, via corresponding capacitive coupling circuits, rendering claim 55 obvious. The capacitive coupling circuit would provide AC coupling and DC blocking, thus helping to minimize false triggering of the switches due to inadvertent type DC biasing that would be coupled with clock output CLKO/Ø.

Claims 20 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imamiya/Pfiffner as applied to claim 18 above, and further in view of Ito et al. (Ito). As previously described, the combination of Imamiya/Pfiffner reads on the basic limitations recited within claim 18. However, the references do not clearly show or disclose circuitry for reducing voltage change rates of the charge pump clock output during both positive and negative transitions. Similar to the reasoning described in some of the previous rejections above, it would have been obvious to one of ordinary skill in the art to utilize Ito's ring oscillator shown in Fig. 12 to provide clock output Ø to Imamiya's circuit. With such a ring oscillator, circuitry 59-61 and 62-64 would reduce the voltage change rates of charge pump clock output CLKO/Ø during both positive and negative transitions, wherein the clock output would be substantially sine-like. This renders claim 20 obvious. The use of Ito's ring oscillator, to provide clock output Ø to Imamiya's apparatus, provides one known type of charge pump clock generating circuit. For example, Ito's circuit is one specific type of a known clock generating circuit/ring oscillator, wherein Imamiya only shows/discloses it in generic ways (e.g. as oscillator 902 in Fig. 2 cited on lines 36-37 of column 1; and as clock generator 2 in Fig. 4 cited on lines 49-51 of column 4).

Ito's circuit provides a stable output clock. Ito's charge pump clock generating circuit 70 comprises circuitry 59-61 and 62-64 that limits current to each amplifying driver circuit (e.g. 51a,51b; 52a,52b; and 53a,53b) within charge pump clock generating circuit 70, and claim 22 is rendered obvious. Each of Ito's discrete capacitive devices 51c-53c 53c is coupled to a corresponding output of an amplifying driver circuit, thus limiting a rate of voltage change of that driver circuit's output. This renders claim 23 obvious.

Claims 50-51 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Imamiya/Pfiffner as applied to claim 49 above, and further in view of Clark, another reference found during the recent search. As previously described, the obvious combination of Imamiya and Pfiffner reads on the limitations of claim 49. However, neither reference clearly shows or discloses the use of a plurality of TC discharging switches, or a plurality of TC charging switches. Fig. 2 of Clark shows one example of a charge pump apparatus comprising a flying capacitor type circuit. However, instead of showing only a single discharging switch for coupling TC 30 to output supply 20b, or a single charging switch to couple TC 30 to voltage source Vs, Clark shows an example of using a plurality of TC discharging switches 42 (i.e. with two series coupled, unlabeled transistors), and a plurality of TC charging switches 34 (i.e. series coupled transistors 70 and 72) coupled to TC 30. Therefore, it would have been obvious to one of ordinary skill in the art to replace Imamiya's single discharging switch QP11 with a plurality of TC discharging switches controlled by clock output CLKO/Ø, as well as replace Imamiya's single charging switch QN11 with a plurality of TC charging switches also controlled by clock output CLKO/Ø, rendering claims 50-51 and 53 obvious. The plurality of series coupled charging switches, and series coupled discharging

switches, would allow each switch within its plurality to drop less voltage across it, thus minimizing the possibility that a high voltage difference would cause any one switch to become damaged, and/not operate effectively. For example, if only one switch (e.g. one single transistor) is used, the full amount would be dropped across it, while if two series coupled switches are used, the full amount would be divided between them, allowing each switch to have only half the full amount across each switch.

Claims 24-25, 27, 60-61, and 66-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imamiya in view of Yamashiro. Fig. 15A of Imamiya shows a charge pump apparatus for generating output voltage supply OUT, wherein the apparatus comprises transfer capacitor C2 for conveying charge from voltage source VDD to output voltage supply OUT; at least one source switching device QN11 disposed between transfer capacitor C2 and voltage source VDD, and having a control node substantially isolated from both transfer capacitor C2 and voltage source VDD (e.g. the gate of QN11 is not coupled directly to either C2 or VDD); at least one output switching device QP11 disposed between transfer capacitor C2 and output voltage supply OUT, and having a control node substantially isolated from both C2 and OUT; and control nodes of the source/output switching devices QN11/QP11 receive charge pump clock output Ø. Although Imamiya does not show or disclose the use of a capacitive coupling circuit for coupling the clock output to the control nodes, one of ordinary skill in the art understands the use of a coupling/blocking capacitor to provide AC coupling/DC blocking. For example, Fig. 1 of Yamashiro shows coupling one single input signal Vin to the control node of a pair of coupling switches Mn,Mp through capacitors C1,C2, respectively, and discloses these capacitors are for AC coupling and DC blocking with respect to sine like waves of an oscillating operation

(e.g. see column 3, lines 9-12 and 55-66). Therefore, it would have been obvious to one of ordinary skill in the art to add a corresponding capacitive coupling circuit between whatever circuitry is providing clock output Ø to Imamiya's circuit and the control node of each of switching devices QN11,QP11, rendering claim 24 obvious. These capacitive coupling circuits would block any unwanted DC component from Ito's charge pump clock generating circuit 70, while still allowing the AC component of clock output Ø to control the transfer capacitor coupling switches at the desired operating frequency. This would minimize any inaccurate triggering of the coupling switches due to unwanted DC biasing. The capacitive coupling circuit(s) would include a first capacitive coupling circuit coupling clock output Ø to the control node of source switching device QN11, and a second capacitive coupling circuit coupling clock output Ø to the control node of output switching device QP11. Therefore, claim 25 is rendered obvious. Since source switching device QN11 (between C2 and VDD), and output switching device QP11 (between C2 and OUT) are each capacitively coupled to clock output Ø via their corresponding capacitive coupling circuit, claim 27 is rendered obvious. Interpreting the combination of Imamiya/Yamashira in another manner, Yamashira's first capacitive coupling network between clock output Ø and the control node of Imamiya's TC charging switch QN11 couples first charge pump clock output Ø to the control node and does not conduct a significant portion of the charge for output OUT, wherein TC C2 is coupled to source voltage VDD during charge periods via TC charging switch QN11 under control of first charge pump clock output Ø (i.e. when high); and Yamashira's second capacitive coupling network between clock output Ø and the control node of TC discharging switch QP11 couples second charge pump clock output Ø to the control node and does not conduct a significant portion of the charge for output OUT,

wherein TC C2 is coupled to output supply OUT during discharge periods, alternating nonconcurrently with the charge periods, via TC discharging switch QP11 under control of second charge pump clock output Ø (i.e. when low). This renders claim 60 obvious. Since second charge pump clock output Ø is first charge pump clock output Ø, claim 61 is also rendered obvious. When each actively controllable TC coupling switch QN11-QN12,QP11-12 of charge pump QN11-QN12,C2,QP11-QP12 is capacitively coupled to receive charge pump clock output Ø, claims 66-67 are rendered obvious. The capacitive coupling, as previously described above, would couple the AC components of clock output Ø to each of the control nodes, while blocking any unwanted DC components of the clock output, thus minimizing inaccurate switching due to possible DC biasing associated with clock output Ø.

Claims 1-2, 4, 9-10, 12-14, 16-17, 28-33, 36-41, and 43-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes et al. (Forbes), another reference found during the recent search, in view of Ito et al. (Ito), one of the references cited in previous Office Actions. Fig. 8 of Forbes shows a charge pump apparatus, for generating output voltage supply VOUT, comprising transfer capacitor 412; plurality of transfer capacitor coupling switches 488-492 coupled to transfer capacitor 412, wherein each switch is effectively switchable between conducting and nonconducting states under control of charge pump clock output Ø (e.g. either directly or indirectly). During periodic first times (i.e. when Ø is high), switches 488-489 are conducting, while switches 491-492 are nonconducting, thus allowing transfer capacitor 412 to charge up by coupling it to voltage source 402. During periodic second times (i.e. when Ø is low) that is not concurrent with the first time, switches 488-489 are nonconducting, while switches 491-492 are conducting, thus coupling transfer capacitor 412 to output voltage supply

VOUT. However, the reference does not show/disclose a charge pump clock generating circuit with a ring oscillator having three inverting driver sections; circuitry for limiting a rate of the voltage rise at a driver section output; and circuitry for limiting a rate of the voltage fall at the driver section output. However, Fig. 11 of Forbes shows a phase/waveform diagram for clock output Ø used within the Fig. 8 charge pump apparatus, and one of ordinary skill in the art would know numerous types of clock generating circuits are available for generating a single phase signal to effectively control the plurality of transfer capacitor coupling switches. Ito shows and discloses one such example in Fig. 12, wherein charge pump clock generating circuit 70 provides single phase signal CLKO. Therefore, it would have been obvious to one of ordinary skill in the art to utilize Ito's charge pump clock generating circuit 70 to provide charge pump clock output CLKO as clock output Ø used to control Forbes' switches 488-492. Ito's charge pump clock generating circuit 70 includes a ring oscillator comprising three inverting driver sections (i.e. 59,51a,51b,62; 60,52a,52b,63; and 61,53a,53b,64) cascaded sequentially in a ring, wherein driver section 61,53a,53b,64 outputs charge pump clock output CLKO, which would correspond to Forbes' charge pump clock output Ø. Each driver section comprises circuitry to limit the rate of rise and fall of voltage at the driver section's output. For example, driver section 61,53a,53b,64 includes: 1) circuitry 61,53a configured as an active current limit to limit the rate of rise of voltage CLKO from a low level to a high level when 53a is turned on, and circuitry 53b,64 configured as an active current limit to limit the rate of fall of voltage CLKO from a high level to a low level when 53b is turned on. This renders claim 1 obvious. The use of Ito's ring oscillator is just one example of a charge pump clock generating circuit/ring oscillator that would provide stable generation of charge pump clock output Ø (i.e. Ito's CLKO). Since each transfer

capacitor coupling switch is controlled by charge pump clock output Ø (e.g. switches 489 and 491 are controlled directly, while switches 488 and 492 are controlled indirectly), claim 2 is rendered obvious. Deeming the line coupling the clock output from Ito's charge pump clock generating circuit 70 to transfer capacitor coupling switches 489 and 491 as coupling circuitry, the clock output will be coupled as a signal to at least one transfer capacitor coupling switch without increasing the rise of voltage rise or fall, thus rendering claim 4 obvious. The current mirror configurations shown in Ito's Fig. 12, which limits source and sink currents conducted by each driver section, will ensure substantially identical magnitudes. For example, the sink currents through transistors 62-64 will correspond to the currents flowing within transistors 56-57, and the source currents through transistors 59-61 will correspond to the current flowing within transistor 58. With transistors 58 and 57 coupled in series between Vdd and Vss, their currents will be the same, and claim 9 is rendered obvious. Since transfer capacitor 412 will be periodically coupled between voltage source 402 and ground in response to charge pump clock output Ø in order to charge, a substantial charge will be coupled into transfer capacitor C2 through 489 during those periods, and with the conducting state of 489 controlled by output Ø, the charge will be via charge pump clock output Ø, thus rendering claim 10 obvious. In another interpretation of Forbes' Fig. 8, one of ordinary skill in the art would consider switches 488-489 as active switches that allow transfer capacitor 412 to be charged when they are turned on, and switches 491-492 as active switches that allow transfer capacitor 412 to be discharged in an alternative, non-overlapping, manner. This would allow transfer capacitor 412 to be coupled alternately between source connection 402 and output connection VOUT. Ito's charge pump clock generating circuit 70 comprises active driver circuit 70 configured to source current (via

61,53a) to, and sink current (via 53b,64) from, charge pump clock output CLKO (of Ito, corresponding to Forbes' clock output Ø). The periodic switching of 488-489 and 491-492 will be provided by a waveform that is substantially sine-like (e.g. not a true square wave) due to the current limiting of 61 and 64, and capacitance 53c. Since clock output CLKO/Ø will be coupled to the gates of Forbes' MOS transistors 489 and 491 (of the plurality of active switches), there will be no substantial charge from clock output CLKO/Ø coupled from source connections 402 to output connections VOUT of transfer capacitor C2. Ito's circuitry 61,53a will limit the source current provided by active driver circuit 70 to clock output CLK0/Ø, and circuitry 53b,64 will limit the current sunk from clock output CLKO/Ø, rendering claim 12 obvious. Discrete capacitive element 53c of Ito's charge pump clock generating circuit 70 is coupled to driver output node CLKO, and will reduce voltage rates of change at that node, rendering obvious claim 13. Since Ito's charge pump clock generating circuit 70 includes a plurality of active driver circuits (e.g. 51a,51b; 52a,52b; and 53a,53b) configured to both source and sink current with respect to a corresponding driver output node, wherein circuitry 59-61 limits the current source capacity to each active driver circuit, and circuitry 62-64 limits current sink capacity in each active driver circuit, claim 14 is rendered obvious. Charge pump clock generating circuit 70 of Ito is a current-starved ring oscillator, and claim 16 is rendered obvious. For the same type of reasoning as applied to claim 9 described above, claim 17 is also rendered obvious since the source current circuitry and sink current circuitry are configured to limit source and sink currents to a substantially identical magnitude. With another interpretation of the Forbes/Ito combination, Forbes' discharging TCCS circuit 492 couples transfer capacitor (TC) 412 to output supply VOUT during discharge periods under control of first charge pump clock output CLKO/Ø (i.e.

when its low); and Ito's 61,53a,53b,64 actively limit a rate of voltage change of the first charge pump clock output CLKO/Ø during both positive and negative transitions such that a voltage of first charge pump clock output CLKO/Ø is substantially sine like (e.g. not a true square wave), rendering claim 28 obvious. Forbes' charging TCCS circuit 489 couples transfer capacitor 412 to source voltage 402 during charge periods under control of second charge pump clock output CLKO/Ø (i.e. when its high) that nonoverlappingly alternate with the discharge periods (e.g. when 489 is off, 492 is on); and Ito's 61,53a,53b,64 actively limit a rate of voltage change of the second charge pump clock output CLKO/Ø, and claim 29 is rendered obvious. Since the first/second charge pump clock outputs correspond to charge pump clock output CLKO/Ø, they are the same clock output, rendering claim 30 obvious. Also, all TCCS circuits 488-492 are effectively controlled by means of charge pump clock output CLKO/Ø, and they are thus all controlled by the first charge pump clock output, rendering claim 31 obvious. When TCCS circuit 489 is conducting, TC 412 is connected to source voltage 402 during the charging period via charge pump clock output CLKO/Ø. This renders claim 32 obvious. Ito's current limiting circuit 61,53a,53b,64 limits current drive capacity of charge pump clock output CLKO/Ø, rendering obvious claim 33. Ito's first clock generator driver circuit 61,53a,53b,64 is a driver circuit functionally incorporated in first clock generator circuit 70, which is configured to generate first charge pump clock output CLKO/Ø. First current limiting circuit 61,53a limits source currents from particular first clock generator driver circuit 61,53a,53b,64; and second current limiting circuit 53b,64 limits sink currents into the particular first clock generator driver circuit, rendering claim 36 obvious. Due to the current mirror relationships of 61 and 64 with 56-58, the source and sink currents will be limited to substantially identical magnitudes, and

claim 37 is rendered obvious. First current limiting circuit 61,53a comprises current mirror device 61 (with respect to current mirror 58-61), and second current limiting circuit 53b,64 comprises different current mirror device 64 (with respect to current mirror 56-57,62-64), thus rendering obvious claim 38. Ito's 59-61 limit source currents, and 62-64 limit sink currents, from all first clock generator driver circuits (e.g. 59,51a,51b,62; 60,52a,52b,63; and 61,53a,53b, 64), and claim 39 is rendered obvious. Since Ito's first charge pump clock output is generated by means of current-starved ring oscillator 70, that includes three inverting driver sections 59,51a, 51b,62; 60,52a,52b,63; and 61,53a,53b, 64 coupled in a ring, claim 40 is also rendered obvious. When conducting and not in any transitioning phase, TCCS circuit 489 couples TC 412 to source voltage 402 passively, and TCCS circuit 492 couples TC C2 to output supply OUT. Therefore, under these conditions (i.e. conducting, and not in any transitioning phase), 489 and 492 will each be one type of a passive TCCS circuit, rendering claim 41 obvious. However, in another interpretation of what can be considered one type of a passive TCCS circuit, 492 does not directly receive clock output Ø. Therefore, it is one type of a passive TCCS circuit that will couple TC 412 to output supply VOUT due to its diode operating characteristics, but still being controlled by clock output CLKO/Ø. This renders claim 41 obvious. In another interpretation of the Forbes/Ito combination, discharging switch circuit 492 couples TC 412 to output supply VOUT under indirect control of first charge pump clock output CLKO/Ø (i.e. when low); corresponding source current limiting circuits 59-61 of Ito limit source current provided to its corresponding driver output node within current-starved ring oscillator 59,51a,51b,62/60,52a,52b,63/61,53a, 53b,64 having three inverting driver stages 59,51a,51b,62; corresponding sink current limiting circuits 62-64 limit sink current drawn from its

corresponding driver output node; and inverting driver output node CLKO of inverting driver stage 61,53a,53b,64 of the first charge pump clock generator is first charge pump clock output CLKO/Ø, rendering claim 43 obvious. TC 412 is coupled to source voltage 402 via charging switch circuit 489, under direct control of second charge pump clock output CLKO/Ø (i.e. when high), during charge periods alternating nonconcurrently with the discharge periods (e.g. only 489 or 492 conducts at a time), and claim 44 is rendered obvious. Capacitor 53c is coupled to driver output node CLKO of the first charge pump clock generating circuit to limit voltage transition rates of driver output node, rendering claim 45 obvious.

Claims 1-4, 10, 12, 14, 16, 43-44, 48, 50-51, 53, and 57-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tasdighi et al., a reference cited in the previous Office Action, in view of Yamauchi, another reference cited in the previous Office Action. Fig. 2 of Tasdighi shows a charge pump apparatus for generating output voltage supply Vout, wherein the apparatus comprises transfer capacitor C1; a plurality of transfer capacitor coupling switches SW1,SW2 with each switch switchable between conducting and nonconducting states under control of a charge pump clock output from charge pump clock generating circuit 24. Coupling switches SW1 and SW2 will each comprise CMOS inverter 26,27 shown in Fig. 3 (e.g. see column 3, lines 37-43), wherein each of transistors 26 and 27 is a distinct transfer capacitor coupling switch. One of ordinary skill in the art would understand the operation of Tasdighi's circuit, which is also described on column 3, lines 16-36. Transfer capacitor C1 charges when switches SW1,SW2 couple the upper terminal of C1 to voltage source Vin and its lower terminal to Gnd; and discharges when the switches couple the upper terminal to Gnd and its lower terminal to output voltage supply Vout. Therefore, one of ordinary skill in the art would know

the transfer capacitor is alternately charged and discharged in accordance with the clock output. The charging would occur during periodic first times, and the discharging would occur during periodic second times that are not concurrent with the first times (e.g. both transistors 26 and 27 within its own respective switch SW1 or SW2 will not be full on, or off, at the same time). Although Tasdighi does not clearly show or disclose charge pump clock generating circuit 2 comprising a ring oscillator with no more than three inverting driver sections, or circuitry for limiting current at a driver section's output, column 5, line 21 cites related "Oscillator 14 could be a ring oscillator". Fig. 5 of Yamauchi shows/discloses charge pump 37 receiving charge pump clock output CLK from charge pump clock generating circuit 39, which is clearly identified as a ring oscillator. Figs. 6 and 7 both show examples of this ring oscillator, wherein each figure shows it comprising at least three inverting driver sections. Therefore, one of ordinary skill in the art would understand Yamauchi provides support for the use of controlling a charge pump with a ring oscillator with an odd number of driver sections, which includes three sections. As such, it would have been obvious to one of ordinary skill in the art to use Yamauchi's ring oscillator 39 to provide its charge pump clock output CLK to the plurality of transfer capacitor coupling switches SW1,SW2 of Tasdighi. Using a version of three inverting driver sections from Yamauchi's Fig. 7, it has circuitry 49 configured as an active current limit to limit a rate of rise of voltage at each driver section's output, and circuitry 47 configured as an active current limit to limit a rate of fall of voltage at each driver section's output. Since the plurality of Tasdighi's transfer capacitor coupling switches will be under control of the particular charge pump clock output CLK (i.e. the output of the final driver section of the ring oscillator), claims 1 and 2 are rendered obvious. The use of a ring oscillator with only three driver sections

requires fewer elements, takes up less area, and consumes less overall current, than a ring oscillator having a higher, odd number of driver sections. Deeming the line coupling the clock output from charge pump clock generating circuit (24 of Tasdighi; Fig. 7 of Yamauchi) to the control nodes of transistors 26,27 as coupling circuitry, the signal will be coupled to each coupling switch without increasing the rise of voltage rise or fall, thus rendering claims 3-4 obvious. Since transfer capacitor C1 will be periodically coupled between voltage source Vin and Gnd in response to the charge pump clock output in order to charge, a substantial charge will be coupled into transfer capacitor C1 during those periods, rendering claim 10 obvious. One of ordinary skill in the art would realize switches SW1 and SW2 of Tasdighi allow transfer capacitor C1 to be charged and discharged in an alternative, non-overlapping, manner. Since a corresponding CMOS inverter of Tasdighi's Fig. 3 can be used for each active switch SW1,SW2, the apparatus of Tasdighi can be interpreted as comprising transfer capacitor C1; active switch 26 can be disposed in series between transfer capacitor C1 and voltage source Vin; active switch 27 can be disposed in series between transfer capacitor C1 and output voltage supply Vout; and charge pump clock generating circuit (of Yamauchi's Fig. 7) comprises active driver circuit 43,45 configured to source current (via 43) to, and sink current (via 45) from, charge pump clock output CLK. The periodic switching of 43 and 45 will provide a CLK waveform that is substantially sine-like. Since clock output CLK will be coupled to the gates of MOS transistors 26,27 (the active switches), there will be no substantial charge from the clock output coupled from the source connections to the output connections of transfer capacitor C1. Circuitry 49 will limit the source current provided by active driver circuit 43,47 to clock output CLK, and circuitry 47 will limit the current sunk from clock output CLK, rendering claim 12 obvious.

Since Yamauchi's charge pump clock generating circuit comprises a plurality of active drivers (each comprising transistors 43 and 45), and circuitry 49/47 for limiting current sourcing/sinking capacities of each active driver circuit with respect to their corresponding driver output node, claim 14 is also rendered obvious. With circuitry 49 and 47, one of ordinary skill in the art would understand that the charge pump clock generating circuit of Yamauchi is configured as a current-starved ring oscillator, rendering claim 16 obvious. Using only three driver stages within Yamauchi's first charge pump clock generator circuit as previously described above, and interpreting the Tasdighi/Yamauchi references in another manner, Tasdighi's transfer capacitor (TC) C1 is coupled to output supply Vout via a discharging switch (e.g. transistor 27 of Fig. 3, with respect to SW2 of Fig. 2); Yamauchi's corresponding source current-limiting circuit 49 limits the source current to each inverting driver output node of each driver stage 43,45; corresponding sink current-limiting circuit 47 limits the sink current drawn from each inverting driver output node; and the inverting driver output node of the last of the three inverting driver stages (of the first charge pump clock generator circuit) is first charge pump clock output CLK. This renders claim 43 obvious. Since TC C1 is coupled to source voltage Vin via a charging switch (e.g. transistor 26 of Fig. 3, with respect to SW1 of Fig. 2) controlled by second charge pump clock output CLK, during charge periods alternating nonconcurrently with the discharge periods, claim 44 is rendered obvious. The lines, going to the control nodes of the transistors 26 and 27 shown within Tasdighi's Fig. 3, are one type of network (e.g. each network comprising a single line), first charge pump output CLK is coupled as a signal to the control node of the discharging switch circuit, and claim 48 is rendered obvious. If one of transistors 26 and 27 of each of SW1 and SW2 is considered a discharge switch, and the other transistor is considered a

charging switch, then there will effectively be a plurality of TC discharging switches, and a plurality of TC charging switches. For example, the charging switches would correspond to those switches coupling C1 between Vin and Gnd, allowing transfer capacitor C1 to charge, wherein the discharging switches would correspond to those switches coupling C1 between Gnd and Vout. Therefore, this plurality of discharging and charging switches render claims 50 and 51, as well as claim 53, obvious. Transistors 49 and 47 of Yamauchi make up circuitry that effectively reduces voltage change rates during both positive and negative transitions of charge pump clock output CLK since those elements reduce, or limit, the amount of current allowed to flow to the output node. Therefore, claim 57 is rendered obvious. Since Yamauchi's charge pump clock generator circuit (shown in Fig. 7) has at least one driver circuit (e.g. each set of transistors 43,45 can be considered a driver circuit), and transistors 49 and 47 limit the currents output from each driver circuit, claim 58 is rendered obvious.

Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tasdighi/ Yamauchi in view of Pfiffner. Related to various rejections previously described above, one of ordinary skill in the art would understand that TC C1 would be coupled to output supply Vout during discharge periods via a TC discharging switch (e.g. 26 will conduct when clock output CLKO/Ø is high); and coupling TC C1 to voltage source Vin via a TC charging switch (e.g. 27 will conduct when clock output CLKO/Ø is low) during charge periods that nonoverlapplingly alternate with the discharge periods. Each of the switches is under control of single-phase charge pump clock output CLKO/Ø. It would have been obvious to one of ordinary skill in the art that single-phase charge pump clock output CLK/Ø is passively coupled (e.g. coupled by an interconnecting line with no intervening elements) to the control nodes of the charging/

discharging switches (e.g. see Tasdighi's transistors 26,27 shown in Fig. 3, with respect to SW1,SW2 shown in Fig. 2), and the gate of each MOS transistor will substantially isolate transfer capacitor (TC) C1 of Tasdighi from Yamauchi's clock output CLK. Therefore, claim 49 is rendered obvious. For example, Pfiffner discloses that "passive elements are...interconnect lines" on column 1, lines 44-45.

Claims 50-51 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imamiya/Ito/Yamashiro as applied to claim 49 above, and further in view of Clark. Applying the same type of reasoning as previously described above with respect to the rejections of claims 50-51 and 53 using only the Imamiya, Ito, and Clark references, claims 50-51 and 53 are again rendered obvious. The plurality of discharging switches and plurality of TC charging switches will provide a means for sharing the voltage drop across the switches within their respective plurality.

Allowable Subject Matter

Claims 11, 21, 42, and 52 are allowed. There is no motivation to modify or combine any prior art reference(s) to ensure: 1) the second control node AC impedance is at least twice the first control node AC impedance as recited within claim 11; 2) the second device area is greater than double the first device area as recited within claim 21; 3) the discharge output TCCS has a control node AC impedance at least double the control node AC impedance of the discharge common TCCS as recited within claim 42; and 4) the second TC discharging switch has a control node AC impedance at least twice as large as a control node AC impedance of the first discharging switch as recited within claim 52 .

Claim 26 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is no motivation to modify or combine any prior art reference(s) to ensure the capacitive coupling circuit includes biasing circuitry that allows an average control voltage to cause a switching device to be substantially nonconductive as recited within claim 26.

Claims 62-65 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is no motivation to modify or combine any prior art reference(s) to ensure the biasing is at some type of average voltage that has not been clearly identified within the claim. Claims 63-65 depend on claim 62.

Response to Argument

The arguments/comments within the Appeal Brief submitted on Jan 8, 2007 were reviewed and considered with the following results.

The applicants' arguments, see the Appeal Brief, filed Jan 8, 2007, with respect to the examiner's use of "could", "could have", "can", and some rejections that did not clearly identify secondary references that would support the examiner's viewpoints, were fully considered and found persuasive. Therefore, all the previous rejections have now been withdrawn. The examiner mistakenly overlooked the apparent fact that the applicants do not appear to rely on common sense and knowledge of technology of what one of ordinary skill in the art understands with respect to prior art, but relies on having everything clearly shown or disclosed, or on phrasing and specific words in attempts to distinguish over known prior art references. Although those previous rejections have been withdrawn, new rejections with different (e.g. improved)

phrasing, and/or including references to support the examiner's reasoning, have been described above. However, it is noted that the new rejections using the Tasdighi et al. reference still cite one use of "could", since Tasdighi clearly discloses "Oscillator 14 could be a ring oscillator" on column 5, line 21.

Another mistake by the examiner was not making any restriction requirement. On page 18 of the Appeal Brief, the appellants "regret the extreme length of this Appeal Brief. No restriction requirement was issued, leaving 65 claims at issue in this appeal." This appears to indicate the applicants admit that the numerous claims contain restrictable material. However, from the examiner's original viewpoint, the claims were deemed similar enough, and well known, that a restriction requirement was not necessary. It was initially believed that after the first Office Action, the applicants would actually begin to concentrate on more critical features of the invention, such as impedance, device area, and capacitive coupling with biasing. However, the applicants' following responses have implied the sine-like clock signals, three stage ring oscillator, current-starved ring oscillator, etc. are apparently critical features of the invention also that one of ordinary skill in the art would not understand even though the original disclosure merely cites "may have a significantly sine-like shape" on page 12 without defining what "sine-like" means, or supporting it with any waveform diagram; shows three inverting driver circuits in Fig. 5 and disclosing it on page 12, without explaining why one (e.g. an odd number) driver circuit would be used, or why an odd number of no more than three driver circuits would not be used; and also cites "Any clock generator may be employed" on page 18. From this examiner's perspective, these statements do not to support any criticality of these claimed features. If the applicants are so intent on stating the references cited by the examiner

lack certain details, why would the applicants' original disclosure be held to a different standard? For example, its disclosure and figures lack support for at least the claimed limitations just described above (i.e. sine-like, and having a ring oscillator will possibly only one inverting stage). Or do the applicants imply that what their disclosure doesn't completely show and disclose would be understood by one of ordinary skill in the art, but references by anyone else must show and disclose all details for one of ordinary skill in the art to understand?

Page 33 of the Appeal Brief shows examples of how Tashighi's switching elements within the charge pump can be configured, and then goes on to describe how and why it would not work properly, and "something more is needed for the circuit to work properly." However, Tasdighi's circuit is similar to Imamiya's Fig. 15A circuit, with one basic different. Tasdighi's charge pump provides a negative pump voltage out since transfer capacitor C1 will be coupled to Gnd during the discharge mode, wherein Imamiya's circuit will provide a positive pump voltage out since it connects transfer capacitor C2 to VDD (via QP12) during the discharge mode. Since both Tasdighi et al. and Imamiya are valid patents, their operation is understood to be functional. If the switching circuits of a flying capacitor type charge pump are so critical, as the applicants appear to imply, it is not understood why so many prior art references merely show generic type switches with arrows, and some of these references do not even show any type of signal(s) controlling them. It is strongly believed that one of ordinary skill in the art will understand how those switches will work, what type of control signal(s) they will require, and how they will provide the proper switching operations during the charge and discharge operations of the flying capacitor type charge pump.

Related to this, the applicants cite "the Examiner consistently fails to consider contrary evidence indicating that such features are not fairly taught by the prior art" on page 22 of the Appeal Brief. In the examiner's defense, the examiner strongly believes that the prior art cited by the examiner, and the knowledge of one of ordinary skill in the art, would be able to provide enough insight into understanding the numerous limitations and variations cited within the claims without having to cite references showing or disclosing every little detail known to those in the art. Also, the examiner strongly believes the applicants fail to consider the evidence clearly shown or disclosed by the prior art cited by the examiner, and also understood by one of ordinary skill in the art. For example, the following references (cited by the examiner in this Office Action, or some previous Office Action) are known, and they show, and/or, disclose:

1) ring oscillators, with three inverting driver sections: see Monk et al.: Fig. 4 and column 3, lines 22-27; Fujioka: Figs. 1, 3, and 5, and column 9, lines 33-35; Gorecki et al.: Fig. 7 and column 7, lines 41-42; Kersh, III: Fig. 7 and column 5, lines 47-50; Chern: Fig. 1 and 6-7 and lines 14-16 of the Abstract; Kimura: section 1 of Figs. 1 and 3; Ito et al.: Fig. 12 and column 1, lines 46-48); Puar: elements 16-20 in the sole figure and column 4, lines 17-18; Rasmussen: Fig. 4's "RING OSCILLATOR (OLD ART)" ; and Hara et al.: Fig. 15 and column 1, lines 25-26);

2) a current-starved type ring oscillator, even if the reference does not cite the label "current-starved": see Fujioka: Fig. 3; Kersh, III: Figs. 5 and 7; Chern: Fig. 3 with respect to Fig. 1; Ito et al.: Fig. 12; Rasmussen: Figs. 4 and 4A; and Hara et al.: Figs. 1, 4-6, 8, and 10);

3) using a ring oscillator to control switching in some type a charge pump (e.g. flying capacitor): see Forbes et al.: Fig. 2 and column 5, lines 16-17; Imamiya: Figs. 2 and 5, and columns 1 (lines 36-37) and 4 (lines 49-50); Yamauchi: Fig. 5; Umezawa et al.: Figs. 5, 11, 13,

14, and 16; Fujioka: Figs. 1, 4, 5, and 7; Kersh, III: Figs. 4 and 5; Chern: Figs. 1, and 6-8; Puar: the sole figure; and Hare et al.: Figs. 13-14;

4) direct control of a charge pump (e.g. flying capacitor) by a clock generating circuit (e.g. VCO or ring oscillator), wherein one of ordinary skill in the art would understand the clock output is used to control a switching element (e.g. transistor) or is coupled to a transfer capacitor: see Forbes et al.: clock output of 54 is provided to 56, which will comprise at least one switching element; Potanin: Figs. 2-4 each show clock output fc coupled to switches controlling at least one flying capacitor; Imamiya: Figs. 5, 7-8, 10, and 15A-15B receiving at least clock output Ø; Yamauchi: clock output CLK is applied to pump circuit 37; Umezawa et al.: Figs. 1, 5, 7, 8-11, 13-14, and 16 show a charge pump controlled by clock outputs Ø and /Ø; Bayer et al.: Figs. 1A shows flying capacitor charge pump 10 receiving clock outputs A and B from the generator in Fig. 1B, and charge pump 26 received the output of VFO 24 in Fig. 2; Gorecki et al.: Fig. 9 has capacitive pump 130 receiving the clock output of VCO 910; van Saders et al.: Figs. 9A, 10-12A having a flying capacitor charge pump receiving clock outputs $\phi 1$ and $\phi 2$; Kersh, III: Figs 1 and 4 with a charge pump receiving the clock output of an oscillator; Chern: Figs. 1 and 6-8 with a charge pump receiving a clock output from a ring oscillator; Puar: the sole figure; and Hara et al.: Figs. 13-14;

5) use of a single-phase clock output that clearly controls at least one charge pump (e.g. flying capacitor): see Forbes: Figs. 2, 6, 8, and 12; Potanin: Figs. 2-6; Imamiya: Figs. 7, 8, 10, and 15A-15B; Chern: Figs. 1, and 6-8; and Hara et al.: Figs. 13-14;

6) use of capacitive coupling, whether clearly described or not: Yamashiro: Figs. 1 and 3; van Saders et al.: Figs. 1-2, 10, and 12A; Weaver et al.: Fig. 1; and Rasmussen: Fig. 4; and

7) an interconnect line being a passive element: Pfiffner: column 1, lines 44-45.

Many of these items are not clearly shown or disclosed in some references since they are so well known and understood by one of ordinary skill in the art. For example, Potanin shows flying capacitor type charge pump section S3,C2,S2 in Fig. 2 being controlled by clock output fc. However, the reference does not clearly show or disclose what comprises the switching elements S2-S3. Since each switching element is controlled by the same single-phase clock output, one of ordinary skill in the art would understand a CMOS type switching element with complementary type operation would work. For example, when one MOS element is turned on to connect the top portion of transfer capacitor C2 to Vdd, the other MOS element is turned off to disconnect the top portion of transfer capacitor C2 from output N3. If the same conductivity MOS elements are used within the switching elements S2-S3, a two-phase single, such as complementary signals, would be required to ensure one connection is off when the other connection is on (e.g. see Fig. 1A of Bayer et al., and Figs. 10-11 of van Saders et al.). With CMOS type switching elements, a single-phase signal will accomplish the same type of complementary on/off operations, and a secondary (or complementary) signal is not required.

From just these examples described above, one of ordinary skill in the art would know many different types of combinations are possible. For example: 1) a charge pump (or flying capacitor) is controlled by some type of a clock generating circuit, wherein that circuit would obviously come from circuitry such as oscillators (e.g. ring oscillators or VCOs); 2) the type of charge pump (e.g. those using only diodes and at least one capacitor; a combination of diodes, switching transistors, and at least one capacitor; or using only switching transistors and at least one capacitor with no diode); 3) depending on the switching elements within the charge pump

(e.g. diode(s), same conductivity transistors, or opposite conductivity transistors) would determine whether a single phase, or a multi-phase (e.g. complementary type signals), clock signal would be used to control the charge pump; 4) a ring oscillator could have three stages, and/or have current limiting/starving circuitry; and 5) the use of an AC coupling/DC blocking type capacitive coupling would be determined by various factors (e.g. area available; noise within the circuit's environment and/or signal; and voltages applied that would inadvertently affect biasing/threshold levels of switching elements). The numerous types of charge pumps and clock generating circuits available provide one of ordinary skill in the art with numerous combinational options. However, the applicants appear to want each reference to clearly show, and/or disclose, every single limitation being claimed, whether it is well known or not. Pages 18-19 of the original disclosure indicate that numerous combinations would be understood by "the skilled person." Therefore, this examiner strongly believes that for any significant progress with the present application to occur, the applicants should begin to concentrate on specific, novel, technical features of the invention that are clearly supported by the original disclosure and figures, without dwelling into (and maintaining) the use of well known circuits, and numerous variations of their combinations, that one of ordinary skill in the art would also clearly understand.

The applicants cite "A sine-like charge pump clock waveform is contrary to the goals and practices of prior art charge pumps" on page 52 of the Appeal Brief, and page 24 cites "A claim term must be considered in accordance with its plain meaning, unless the Applicants clearly indicate a contrary intent." If this is the case, what is the "plain meaning" of the applicant's use of "sine-like", and if "sine-like" is so critical to the applicants' invention, why wasn't it clearly

defined and shown in the original disclosure? Even after considering the comments beginning on page 51 of the Appeal Brief, the examiner still requests the applicants to provide a clear definition, and also show examples (e.g. waveforms) of what is, and what is not, considered "sine-like." Without clear, documented support, it is still not understood what this "sine-like" signal looks like; if it can only be provided by the specific current-starved ring oscillator shown in the applicants' own Fig. 5; or if it can be provided by other structures. For example, page 51 of the Appeal Brief cites "nearly rectangular, slightly trapezoidal waveforms" and "nearly square outputs waveforms", and implies that these are not "sine-like." However, the applicants still do not clearly explain what type of waveforms the applicants actually consider as being "sine-like." Adding to this confusion of what is "sine-like", Fig. 11 of Forbes et al. shows a phase/clock timing diagram that is generated by some type of a clock generating circuit (e.g. 54 of Fig. 2, which is disclosed as being a ring oscillator on column 5, lines 16-18). Although the rising and falling edges of the clock signal have slopes, forming a trapezoidal type waveform, the reference is silent on whether this signal is a square wave, sine-like, or some other clear identifier. Monk et al. shows a 3-stage ring oscillator in Fig. 4, with Fig. 5 showing its related waveforms. Monk also discloses that the higher the value of gain of the stage, the more the waveform moves away from a sinusoid, and "a ratio of m close to 2 produces a substantially sinusoidal output" on lines 57-64 of column 1. Although these signals can be considered "sine-like", this is achieved by the widths of the transistors within the ring oscillator shown, instead of the number of inverter stages within the ring oscillator, or the use of current starving/limiting circuitry, that appears to be so critical to at least some of the applicants' claims. Fig. 4 of Chern shows a waveform provided by an inverter, related to a 13-stage ring oscillator shown in Fig. 1, and disclosed as a "square-wave

oscillating signal" on lines 8-9 of column 2. However, with the non-linear rising and falling edges, one of ordinary skill in the art would not consider this signal as a true square-wave. Also, it is strongly believed that Chern's waveform would correspond to what the applicants' own Fig. 5 current-starved ring oscillator would provide as clock output CLK. For example, when the applicants' pull-up section of inverter 506 is turned on, the current through current source 512 will initially begin to quickly charge capacitor 526, but as the voltage charge across the capacitor increases, it will slowly begin to round off as its voltage nears its high level. Similarly, when the pull-down section of Chern's inverter 506 is turned on, the charge across capacitor 526 will initially be discharged quickly via current source 518, but as the capacitor's voltage charge approaches the common potential (i.e. 404), the discharge will slow down to round off eventually at a low potential. Therefore, if the applicants' own ring oscillator will provide the same type of signal as Chern's circuitry, what makes the applicants' "substantially sine-like" signal CLK patentably distinct over Chern's "square-wave oscillating signal"? To help understand this difference, it is suggested the applicants provide a clear example of a waveform that would be provided by the applicants' own Fig. 5 ring oscillator as clock output CLK. Kimura shows output B of a 3-stage ring oscillator (e.g. see 1 in Fig. 2) having linear rising and falling edges, again a trapezoidal type signal. However, Kimura simply identifies it as "a pulse signal" on lines 27-29 of column 3. The applicants may argue that a pulse is not a sine-like signal. However, until the applicants supply a clear definition and example of what is a sine-like signal, the applicants own clock output CLK would also not be considered a sine-like signal since a clock is typically identified with square wave type pulses. Although Rasmussen does not show the output waveform of the three-stage "RING OSCILLATOR (OLD ART)" of Fig. 4,

Rasmussen discloses "Output buffer GI amplifies and squares the ring oscillator signal" on lines 44-45 of column 4. Since the ring oscillator signal is squared, the ring oscillator signal can be considered "sine-like." However, for further clarification in an attempt to still determine what the applicants mean by "substantially sine-like", it is requested that the applicants identify which of the above references clearly shows or discloses signals that are "sine-like", and which of the signals are not "sine-like", with respect to the applicants understanding of "sine-like", and to also clearly explain how "sine-like" and non-sine-like waves are distinguishable from one another. Although the applicants cite the Hara et al. reference with a current-starved ring oscillator of no less than five inverter stages, that reference is not cited in any of the present claim rejections with respect to the sine-like limitations. However, other known references show and disclose 3-stage ring oscillators that correspond to the applicants' own Fig. 5 current-starved ring oscillator structure, and there is nothing preventing those references from being used to reject claims, with respect to the knowledge of one of ordinary skill in the art. Without any clear definition and waveform examples provided by the applicants, it is strongly believed that the applicants are merely relying on the "sine-like" label to distinguish over prior art cited by the examiner, and understood by one of ordinary skill in the art.

Page 18 of the original disclosure cites "Any clock generator may be employed" and "the skilled person may apply aspects of the method and apparatus described herein to a staggering variety of charge pump configurations", and page 19 cites "The skilled person will understand that various omissions, substitutions, and changes in the form and details of methods and apparatus illustrated may be made without departing from the scope of the invention." and "each described element in each claim should be construed as broadly as possible, and moreover

should be understood to encompass any equivalent to such element insofar as possible without also encompassing the prior art." From this examiner's viewpoint, and knowledge of the numerous prior art references available (e.g. the examples described above), the applicants apparently want a one-way street, wherein one of ordinary skill in the art would not find variations of other prior art references obvious over the present application's claims. The numerous claims, arguments, and prior art references submitted by the applicants are viewed by this examiner, and other examiners that have been consulted, as one way to burden the examiner down with so much data (and/or trivia) that the examiner will eventually allow material that is neither novel nor patentable.

All the other arguments of the applicants have been considered, but are moot in view of the new, or modified ground(s) of rejection, which more clearly support the examiner's reasoning for rejecting the claims.

It is also noted that although numerous prior art rejections were described above, many more rejections could have been made due to the well known use of: 1) ring oscillators providing at least one clock signal to a charge pump type circuit; 2) ring oscillators comprising three inverting driver stages, and/or current starving (e.g. current limiting) type structures; 3) charge pump circuits utilizing a flying capacitor type structure, wherein the switching can be controlled by either a single phase clock signal, or a multi-phase type signal (e.g. complementary signals or non-overlapping signals); 4) use of capacitive coupling for AC coupling and DC blocking; and 5) what can be considered sine-like type signals.

Therefore, the rejections cited in this **NON-FINAL** Office Action are deemed proper with respect to the broadest reasonable interpretation of the claimed limitations, and what is known and shown in prior art references.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention, since they show or disclose what is already well-known to one of ordinary skill in the art. Potanin shows examples of a plurality of flying capacitor type charge pumps controlled by a single-phase clock output (e.g. see Fig. 2). Umezawa et al. shows an example of generic ring oscillator (box) 15 applying its clock outputs directly to charge pump 11 (e.g. see Fig. 5). Bayer et al. shows a generic clock generator applying its clock outputs to the same conductivity MOS transistors within flying capacitor type charge pump 10 (e.g. see Figs. 1A-1B). Weaver et al. shows capacitive coupling 23 in Fig. 1 and discloses its capacitance is negligible at the operating frequency (e.g. see column 4, lines 49-52). Monk shows an example of a three-stage ring oscillator in Fig. 4 that provide sinusoidal outputs shown in Fig. 5. Fujioka shows an example of a current-starved ring oscillator in Fig. 3, discloses it can comprise three inverters, and it can be used to control flying capacitor/charge pump 20 shown in Figs. 1 and 5. Gorecki et al. shows a three-stage ring oscillator in Fig. 7 that can be used as VCO 910 in Fig. 9 that provides its clock signal to capacitive pump 130; discloses "the output signal of any of inverters 701-703 approximates a square wave" on column 7, lines 44-45; and different implementations of the capacitive charge pump may be used on column 10, lines 2-3. The reference of van Saders shows various examples of flying capacitor type charge pumps including the use of four same conductivity type MOS transistors in Fig. 10 and the use of

two same conductivity type MOS transistors in Fig. 11, along with two diodes; also capacitive coupling is shown in at least Fig. 1; and at least one biasing type structure 182 is shown in at least Fig. 10. Kersh, III shows an example of current-starved ring oscillator 44 that applies its clock output 45 to charge pump 46 in Figs. 4-5, and discloses a ring oscillator can have three inverter stages on column 5, lines 47-50. Chern shows/discloses a current-starved type ring oscillator in Figs. 1 and 3, with a clock output shown in Fig. 4 that is not a true square wave, and discloses the number of odd inverter stages depends on delay and desired frequency (e.g. see column 1, lines 25-31). Kimura shows an example of three-stage ring oscillator 1 in Figs. 1 and 3, and shows its clock output B is not a true square wave. Puar shows a three-stage ring oscillator with its clock outputs coupled directly to a charge pump in the sole figure. Rasmussen shows capacitive coupling at the output of a three-stage "RING OSCILLATOR (OLD ART)", wherein its output must be sine-like since it needs to be squared by output buffer GI (e.g. see column 4, lines 44-45). Given enough time, the examiner would be able to find and cite additional references that further supports the examiner's rejections described above. Although none of these references clearly show and disclose every limitation recited, one of ordinary skill in the art would understand that numerous variations in combining the references could obviously be made that would read on those limitations. Therefore, all of these references should be carefully reviewed and considered with respect to the broadest reasonable interpretation of the claimed limitations, and what is shown and understood by one of ordinary skill in the art with respect to the prior art.

The prior art references cited on the IDS submitted previously on May 15, 2006 have also been reviewed and considered now. Of the 38 references cited, only six mention a ring

oscillator; none cite current-starving; six cite current limiting; and only one cites something related to sine-like (e.g. sinusoidal or sine-wave). Also, most of these references do not clearly show a flying capacitor type charge pump, and even when a charge pump is shown, either a generic type clock generator/oscillator block is shown, or the clock signals controlling the charge pump are not shown as being provided by any generator/oscillator (i.e. they are provided by some unknown circuitry not shown within the figures). Even in the references that do show flying capacitor type charge pumps, the switching operations are usually controlled by complementary signals (e.g. a two-phase single). Therefore, none of these cited references are considered more significant that the examples described by the examiner above. Those examples more clearly show and disclose circuitry with respect to flying capacitor type charge pumps, ring oscillators, single-phase control, and oscillator clock output signals. [Note: A typo was corrected on reference 10 if the IDS, wherein the issued patent shows the inventor's name as Hausmann instead of Hausman.]

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal, can be reached on (571) 272-1769.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

3 May 2007

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800